In the Claims:

Please amend claims 1, 2, 3, 17 and 19. The claims are as follows:

1. (Currently amended) A structure, comprising:

an FPGA (Field-Programmable Gate Array) including a plurality of FPGA elements, each of the FPGA elements comprising an FPGA CLB (Configurable Logic Block),

wherein each FPGA element in the FPGA is assigned an address and is configured to provide its address, wherein a first subset of the FPGA elements is configured to form a first functional block, wherein the first functional block comprises a mapped location register residing in one or more FPGA CLBs of the first functional block, and wherein the mapped location register ~~is configured to receive and~~ stores the address of a current location FPGA element, the current location FPGA element being in the first functional block and the address of the current location FPGA element being specified as the location of the first functional block.

2. (Currently amended) The structure of claim 1, wherein the first functional block further comprises a mapped destination register residing in one or more FPGA CLBs of the first functional block, and wherein the mapped destination register ~~is configured to receive and~~ stores the address of a destination FPGA element, the address of the destination FPGA element being specified as the destination of the first functional block.

3. (Currently amended) The structure of claim 2, wherein the first functional block further comprises a mapped movement register residing in one or more FPGA CLBs of the first functional block, and wherein the mapped movement register ~~is configured to receive and~~ stores

the direction and distance of a next step of the movement of the first functional block.

4. (Original) The structure of claim 3, wherein the first functional block further comprises a mapped logic location function configured to calculate the direction, distance, and time for the next step of the movement of the first functional block based on the contents of the mapped location register, the mapped destination register, and a time limit allowed for the movement of the first functional block.

5. (Original) The structure of claim 1, further comprising a first localized IO (Input/Output) circuit and a second localized IO circuit both electrically coupled to the FPGA,

wherein the first functional block is formed via the first localized IO circuit, and wherein the first functional block is configured to move to the second localized IO circuit.

6. (Original) The structure of claim 5, wherein the first functional block is configured to move to the second localized IO circuit within a time limit in terms of clock cycles.

7. (Original) The structure of claim 5, wherein a second subset of the FPGA elements are configured to form a second functional block separate from the first functional block at any time, wherein the second functional block is formed via the first localized IO circuit, and wherein the second functional block is configured to move to the second localized IO circuit.

8. (Original) The structure of claim 1, wherein the FPGA further comprises connections

electrically coupling each FPGA element to surrounding FPGA elements such that the contents of all FPGA elements in a functional block can be transferred to their non-adjacent FPGA elements in one clock cycle.

9. (Original) A method for operating an FPGA, the method comprising the steps of:

providing an FPGA including a plurality of FPGA elements, each of the FPGA elements comprising an FPGA CLB wherein each FPGA element in the FPGA is assigned an address and is configured to provide its address;

forming a first functional block on a first subset of the FPGA elements;

providing in the first functional block a mapped location register residing in one or more FPGA CLBs of the first functional block; and

using the mapped location register to receive and store the address of a current location FPGA element, the current location FPGA element being in the first functional block and the address of the current location FPGA element being specified as the location of the first functional block.

10. (Original) The method of claim 9, further comprising the steps of:

providing further in the first functional block a mapped destination register residing in one or more FPGA CLBs of the first functional block; and

using the mapped destination register to receive and store the address of a destination FPGA element, the address of the destination FPGA element being specified as the destination of the first functional block.

11. (Original) The method of claim 10, further comprising the steps of:

providing further in the first functional block a mapped movement register residing in one or more FPGA CLBs of the first functional block; and

using the mapped movement register to receive and store the direction and distance of a next step of the movement of the first functional block.

12. (Original) The method of claim 11, further comprising the steps of:

providing further in the first functional block a mapped logic location function; and

using the mapped logic location function to calculate the direction, distance, and time for the next step of the movement of the first functional block based on the contents of the mapped location register, the mapped destination register, and a time limit allowed for the movement of the first functional block.

13. (Original) The method of claim 9, wherein the step of forming the first functional block on the first subset of the FPGA elements comprises the steps of:

providing a first localized IO (Input/Output) circuit and a second localized IO circuit, both electrically coupled to the FPGA; and

forming the first functional block via the first localized IO circuit.

14. (Original) The method of claim 13, further comprising the step of moving the first functional block to the second localized IO circuit within a time limit in terms of clock cycles.

15. (Original) The method of claim 13, further comprising the steps of:

forming a second functional block on a second subset of the FPGA elements and via the first localized IO circuit, the second functional block being separate from the first functional block at any time; and

moving the second functional block to the second localized IO circuit within a time limit in terms of clock cycles.

16. (Original) The method of claim 9, further comprising the step of providing connections electrically coupling each FPGA element to surrounding FPGA elements such that the contents of all FPGA elements in a functional block can be transferred to their non-adjacent FPGA elements in one clock cycle.

17. (Currently amended) A method for operating an FPGA, the method comprising the steps of:

providing a plurality of FPGA elements, each of the plurality of FPGA elements comprising an FPGA CLB and being assigned an address;

forming a first functional block comprising one or more FPGA elements of the plurality of FPGA elements;

forming a mapped location register residing in one or more FPGA CLBs of the first functional block;

loading the mapped location register with an address of a current location FPGA element, wherein the current location FPGA element is in the first functional block, and wherein the

address of the current location FPGA element is specified as the location of the first functional block; and

moving the first functional block to a destination in the FPGA; and

forming a second functional block comprising at least one FPGA element of the plurality of FPGA elements, the second functional block being separate from the first functional block at any time.

18. (Original) The method of claim 17, wherein the step of forming the first functional block comprises the step of assigning all the FPGA elements of the first functional block a unique function number.

19. (Currently amended) The method of claim 17, further comprising:~~claim 18 wherein the step of forming the first functional block comprises the steps of:~~

~~forming a~~ mapped location register residing ~~in one or more FPGA CLBs of the first functional block;~~

forming a mapped destination register residing in one or more FPGA CLBs of the first functional block;

~~loading the mapped location register with the address of a current location FPGA element, the current location FPGA element being in the first functional block and the address of the current location FPGA element being specified as the location of the first functional block;~~

and

before moving the first functional block to the destination in the FPGA, loading the mapped destination register with the address of a destination FPGA element, the address of the destination FPGA element being specified as the destination of the first functional block.

20. (Original) The method of claim 19, the step of moving the first functional block to the destination in the FPGA comprises the steps of:

forming a mapped logic location function in the first functional block; and

using the mapped logic location function to calculate the direction, distance, and time for the next step of the movement of the first functional block based on the contents of the mapped location register, the mapped destination register, and the time limit allowed for the movement of the first functional block; and

moving all the FPGA elements having the unique function number according to the calculated direction, distance, and time for the next step.